

Viterbi-Like Algorithm for Bit Allocation in Fixed-Point Fast Fourier Transform

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Abstract

With the popularity of Orthogonal Frequency Division Multiplexing (OFDM), fixed-point fast Fourier transform (FFT) has become increasingly important in communication IC design. Ying-Jui Chen et al. proposed a Quasi-Coordinate-Descent-Based (QCDB) algorithm which could be applied to design a fixed-point FFT. In this paper, I used and improved the QCDB algorithm to optimize the signal-to-noise ratio (SNR) for fixed-point FFT. Given the constraint of the available number of bits on an IC chip, the proposed algorithm found the optimal allocation of bits for each twiddle factor to maximize the SNR. First, it described a method to systematically estimate fixed-point FFT noise propagation performance. By modeling the signal and noise propagation in each processing stage of the FFT as a series of signal amplifier stages combined with additive noise sources, it could obtain SNR associated each FFT stage given a certain number of bits. Then, with the SNR for each FFT stage known, this paper proposed the Viterbi-like algorithm to improve the QCDB algorithm which was with the local optimal and to find the global optimal allocation of bits to maximize the SNR. This new modified algorithm was called as Viterbi-like modified quasi-coordinate-descent-based algorithm and showed that it gave the much better result than by the QCDB algorithm through the experiments.

Keywords: twiddle factor, allocation of bits, signal-to-noise ratio.

1. Introduction

With the popularity of Orthogonal Frequency Division Multiplexing (OFDM) (Bohge, Gross, Wolisz, & Meyer 2007; Jiang, Luo, Tian, & Song, 2005; Kim, Kwak, Choi, & Lee, 2004; Zhang & Letaief, 2004), fixed-point Fast Fourier transform (FFT) (Brigham, 1988) has become increasingly important in communication IC design. In an IC, fixed-point FFT implementation is more cost-effective than floating-point FFT. If we can implement the fixed-point FFT using appropriate bit-length for each twiddle factor, the architecture can be even simpler and cheaper to make. Most bit allocation algorithms can be classified into two categories: incremental allocation (Fox, 1966; Hughes-Hartog, 1989; Wyglinski, Kabal, & Labeau, 2002, 2003; Noreen & Baig, 2013), and bit error probability expression-based allocation (Fischer & Huber, 1996; Goldfeld, Lyandres, & Wulich, 2002; Gurung, 2010; Wen, Cheng, Yin, Yang, & Jiao, 2013). The first type of algorithm incrementally allocates an integer number of bits while the other type uses closed form expressions of performance measures in order to determine a non-integer bit allocation and then round the results. On the other hand, bit allocation algorithms can also be classified according to the objective functions they are attempting to optimize.

For a fixed-point implementation, it is inevitable that round-off noise will come into play and maximize the signal-to-noise ratio (SNR) is paramount. In this paper, I decompose the FFT into a series of amplifier stages combined with additive noise that is able to estimate the FFT SNR and is shown in Section 2.1, and then I propose an algorithm to design a fixed-point FFT with maximum SNR given the constraint of the available number of bits for the twiddle factor. Though, if we use the ASIC to implement the algorithm, we can allocate the bit-length for each twiddle factor individually according to the requested precision. Therefore it is a challenge to decide how many bits are better for each twiddle factor.

2. Methods

In the field of digital signal processing, the more bit-length will get the more precision of the signal processing, but relatively it will increase the complexity of the hardware as well as decrease the

computation efficiency. Therefore, it is a tradeoff to decide the suitable bit-length for the system. In fixed-length architecture, there are two quantization methods, round-off and truncation (Albert, 1994; Parhi, 1999) to deal with the problems caused by overflow. Because of the quantization, it introduces the error called quantization noise error. I develop two noise propagation models based on the quantization methods as derived as the following section and use these two models for the FFT to deal with the bit allocation.

2.1. Noise propagation models

The round-off error in quantization noise e_R is modeled as a uniform random variable between $-q/2$ and $q/2$. Therefore, it has the probability density function (pdf) as follows,

$$P_R(e_R) = \begin{cases} 1/q, & |e_R| \leq q/2 \\ 0, & |e_R| > q/2 \end{cases}, \quad (1)$$

where the mean $E(e_R)$ is equal to 0, the $E(e_R^2)$ is equal to $q^2/12$, and the variance $Var(e_R)$ is equal to $q^2/12$.

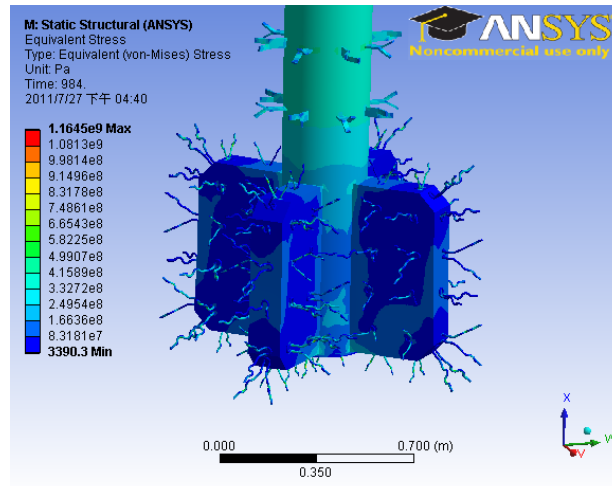


Fig. 1 Data path of crossadder.

In Fig. 1, the input signals are x_1 and x_2 with the additive noise n_{x1} and n_{x2} respectively and the output signal is y with the additive noise n_y .

Table 2 Maximum and minimum temperatures in KR impellers

	Temp. after 30 times		Temp. after 90 times		Temp. after 180 times	
	Min.(°C)	Max. (°C)	Min. (°C)	Max.(°C)	Min. (°C)	Max.(°C)
Y-Type anchor	547	213	386	635	638	903
V-Type anchor	538	115	203	793	462	881

3. Experimental Results

I took the twiddle factor in the first stage of 64-point radix-4 FFT to demonstrate how the proposed algorithm worked. The noise propagation model I used in this experiment was the round-off error in quantization, since we could obtain the $E(e_R^2)$ is equal to $q^2/12$ by the equation (1) for the round-off error model and the $E(e_T^2)$ is equal to $q^2/3$ by the equation (2) for the truncation error

model. Then,

$$10 \log \frac{E(e_R^2)}{E(e_T^2)} = 10 \log 4^{-1} \cong -6dB$$

4. Conclusions

In this paper, it decomposes the FFT butterfly computation into a series of signal amplifier stages combined with additive noise source. By this model, we can estimate the SNR under different bit-length of the twiddle factor fast and systematically. In experiments, it can get the optimal system performance by VLMQCD algorithm than by OCDB algorithm. According to this result, we can choose the optimal solution for the system design. In conclusion, the methods proposed in this paper can decide the bit allocation of the twiddle factor in fixed-point FFT with optimal SNR.

Nomenclature

C specific heat (J/kg·K)

E Young's Modulus (N/m²)

h convection heat transfer coefficient (W/m²·K)

α thermal expansion coefficient (1/K)

ρ density (kg/m³)

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南開學報投稿須知

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摘 要

中文摘要二字採 14 號字體加黑置中，以不超過 500 字為原則（內容宜含目的、方法、結果與結論），摘要後，另起一行，全部以一段式呈現，並含 3~5 個關鍵詞，關鍵詞字樣採 12 號字體加黑，不得與題目中的名詞重複。英文摘要應與中文摘要一致，Abstract 一字以 Times New Roman 14 號字體加黑置中。一般性的論述可用現在式呈現，但有關論文的部分則須以過去式的時態呈現。

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