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Wafer Scale Rerouting Process in making Known Good Dies

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Abstract

To design and make Known Good Dies (KGD) on a wafer prior to packaging, it requires I/O pads to be fanned out through channelized rerouting process. We use the Boundary Scan Test (BST) protocol as verse to the conventional AC/DC type analogue test, to drive and sense each die in accordance with the IEEE1149 standard. By taking advantage of their dicing streets and alleys, this proposed method is to embed test signals such as Test Data Input (TDI), Test Data Output (TDO), Test Mode Selection (TMS) and Test Clock (TCK) into the test channels. The basis of this proposed method is to check each die if recognized by its ID code which resides in its registers. Once the die is passed the ID test, it is prepared to be bumped at different pad locations so called redistribution process. A new geometry of foot-prints are given birth to a finished flip-chip, and these flip-chips are tested again in a module on system level, and thus to minimize the redundant tests and packaging.

Keywords: Flip Chips, Re-routing, Boundary Scan Test, JTAG, KGD, WSI

1. Introduction

This method is to use the thin-film based technology coupling with the boundary scan test signals to redistribute the existing I/O pads from the peripheral to land grid array. It is developed to take advantage of the unused dicing streets in order to carry out the test signals relocated in the avenues, specifically are TDI, TDO, TCK and TMS, of which are generally available to the modern ICs. Upon execution, they are instructed to drive and sense boundary scan cells so called silicon nails on the pins, and these pins are accessible to the outside world, i.e., a JTAG boundary scan controller. Both devices under test and JTAG controller are required to follow up their Boundary Scan Descriptive Language (BSDL), and which are the specified instructions. These instructions usually defined as Instruction, Data, bypass, Capture, etc. registers in order to run

infrastructural and interconnection test besides in system programming.

This test method is known to the PCB industry for years, but not to the microelectronic systems due to bare dies are not easily accessed; for examples, chip-lets and chip-tiles, etc. In recent years, Joint Test Action Group (JTAG) has launched cell-based Infrastructure and Interconnection test on dies, to test micro bumps, Silicon Thru Vias (STV), flip-chips, passive substrates, stack-up dies, etc. assemblies. Once the die is passed by the JTAG based tests, and checked by the boundary scan-based diagnostics (BSD), potential flaws such as open, short, bridging and grounding, etc. manufacturing defectives are ironed out, the next step shall prepare for system level integration like Multi-Chip-Modules (MCM), Chip Scale Packages (CSP), System in Chip (SiP) etc., to run the system level test accordingly.

This enabling technology shall solve many problems involved in microelectronic systems; for instance, a well-known researcher who is Gabriel Loh coworking with Edwards Rogers at the Department of Electrical and Computer Engineering of The University of Toronto, Canada, incorporated with AMD, other research on Chips on Wafer on Substrate (CoWoS) led by Dr. David Hu at National Taiwan University's College of Engineering, who has involved in IC packaging by flip-chips based bumping process, and proven on homogeneous integration and heterogeneous integration upon the fine pitch "copper bumps".

Additional research conducted at The Institute of Microelectronics (IME) at National University of Singapore (IME) who has proposed cost effective interposers for wafer level heterogeneous integration similar to the HMB2, of which using "active silicon interposer" to free off TSV in the CPU/GPU assembly, as verse to NTU's "passive interposer".

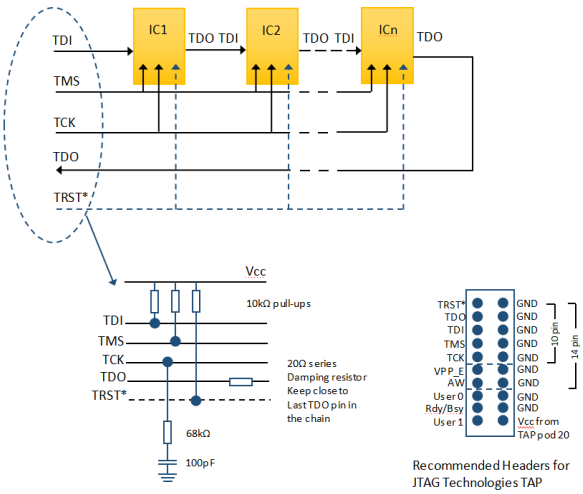
However, many have doubted about 3D integration whether is an opportunity or just a hype; questions raised by Professor: Ji-Fu Li at National Central University and C.T. Wu at Industrial Research Institute (ITRI), they concern about MCMs related Design For Test (DFT), also inquired by Cheng-Wen Wu at National Tsing-Hua University, concerning bandwidth at the chip I/O's, internal TSV's and substrates. Specifically, issues like at-speed test, and higher thermal stresses, etc, causing yielding rate related problem in a multiple factor of $Y_{3D\text{-}W2W} = (Y_{2D})^{n}(Ys)^{n-1}$ where Y is representing yielding of wafer scale integration. Together with Dr. Erik Marinissen's theory in Known Good Dies (KGD as well as Known-Good-Stack (KGS), who has expressed his concerns on the difficulties making System-In-Chip (SiP) when incrementally stacking up foreign objects into fabrications without probation. On the other hand, CMOS based testing methods introduced at the Computer Science Department of The Anna University, home for the IEEE1149 boundary scan test labs, they have studied the importance of using the test pattern generation, fault models, logic verification, Build-In-Self- Test (BIST), compact JTAG (cJTAG), at their labs to ensure reliability of microelectronic assemblies.

2. Methods

2.1 Approaches of Wafer Scale Boundary Scan Test

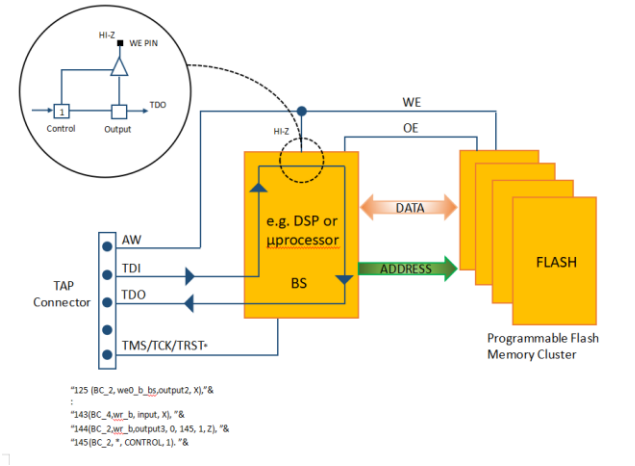
This paper proposed wafer level test is to embed the boundary scan test in line with wafer fab practice, through rerouting process to conduct self-test at each chip if they are they are boundary scannable, ICs.

Those whom making boundary scan IC's like AMD and Intel and Micro, etc., have quipped with the TAP ports, to allow TDI, TDO, TMS, TCK based test signals arranged in a daisy-chain through multiple dies, and some are allowed to bypass one over one another according to IEEE1149 spec., the JTAG based tools are developed to cater those conditions, the arrangement is explained in picture 1;



Picture 1. Boundary Scan based TAP port (Courtesy of JTAG Technologies)

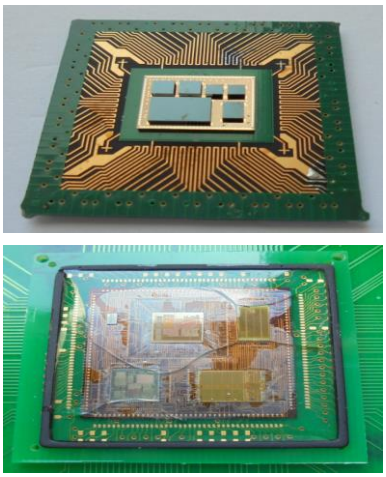
Continuing on picture 2, reveals a typical Test Access Port (TAP) how to access the master chips via CPU, GPU, DSP, etc. active devices in relation to their peripheral memory chips, usually a bank of cache memories like DDR's or temporary data storage devices like SRAM, code storge in the EEPROM, Such a subsystem is depicted as following picture 2;



Picture 2. Boundary scan testing daisy chained dies (Courtesy of JTAG Technologies)

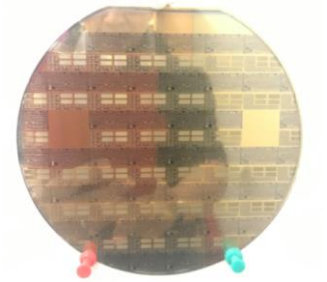
2.2 Method of test specimen in examples

Another example in picture 3, depicts a typical multiple tiles based modular assemblies in 2D, of which debuted before the Boundary Scan Test was prevail, well-constructed but lacking testability, but they are not boundary scan compatible Ic's. and not possibly tested on die level, when the chips were not in compliance with the Boundary Scan Descriptive Language (BSDL) protocol at each I/O registers, i.e., they were "dumb modules";



Picture 3. Prototyping Flip Chip based Multi-Chip-Module (Courtesy of JTAG Technologies)

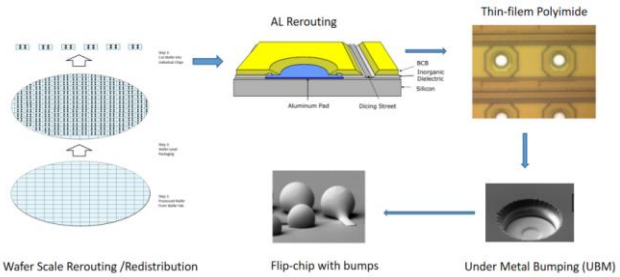
More in picture 4, test experiment made on a bumped wafer, a number of NAND flashes populated on this specimen, and this wafer is prepared to conduct subsequent boundary scan test and programming, once the thin-film based re-routing process is completed as flows;



Picture 4. Prototyping Wafer Scale Bumping (Courtesy of TamKang University)

2.3 Method of transformation of a die from a wafer to flip-chips

In picture 5, it illustrates a standard thin-film based process making bumps in three steps, to relocate from Line of Centre (LOC) to Pin-Grid -Array (PGA), and bumps are fanned out to flip-chip based configuration, as illustrated in the following Wikipedia data base as well as cited in the section of reference materials;

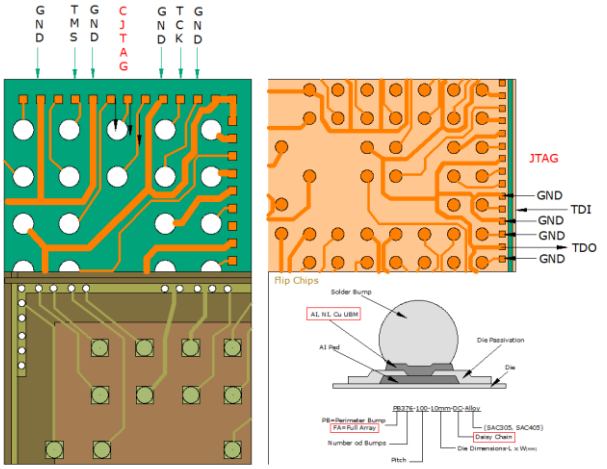


Picture 5. Illustrated exemplary thin-film process in the public domain literature

2.4 Method of thin film process with provision of Test Access Port (TAP)

Rerouting I/O pads from the peripheral to an array of re-distributed bumps, they are buffered and re-arranged to make Test Access Port (TAP) available to the test POD. There are two avenues in X-Y coordinates, the POD has TDI and TDO with shielded by groundings of which are placed serially in rows, while the TCK, TMS are placed in parallel in columns with groundings as well, and the BGA solder balls are daisy chained with notations at each ball; in other words, they are testable as a

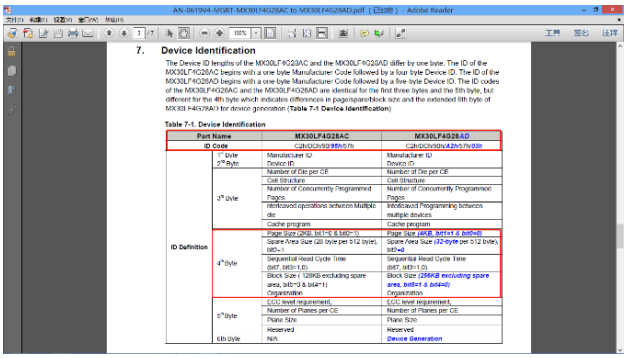
node, i.e., to examine the continuity of a metal formation in construction of Al-Ni-CU based solder bump whether is intact, of which is a common practice in the industry, the baseline illustrated as following picture 6;



Picture 6. Illustrated examples of bumping process in rerouting

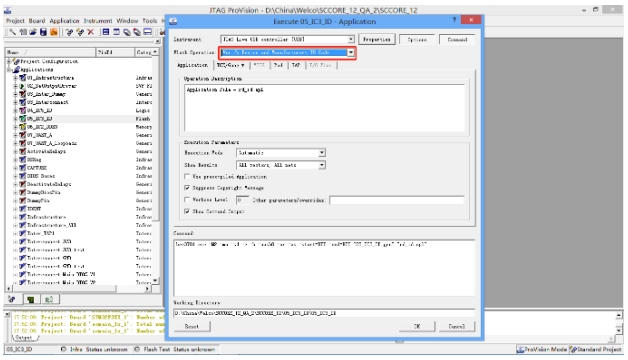
2.5 Method of test environment related measurements in simulation

In picture 7, depicts a flash memory-based application under taken measurements of its device ID, of which covers manufacturing ID, device ID, number of the Die, cell structure, number of concurrently programmed pages, interleaved programming between multiple devices, cache program, page size, square area size, etc. plus sequential read cycle time, block size, organization, ECC level requirement, number of planes per CE, plane size, and the 6th byte of device generation, all of test parameters as shown in the following red marked functionalities.



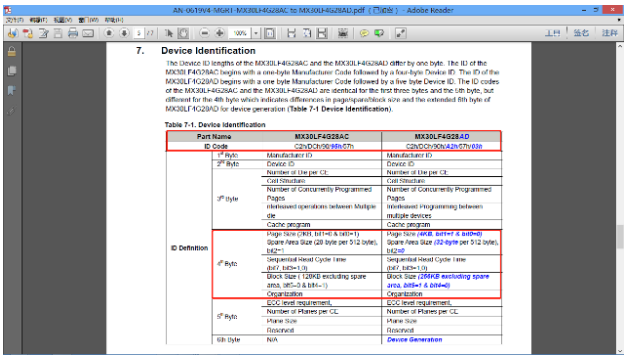
Picture 7. Spec. of a Flash memory with device identification

In picture 8, JTAG performs boundary scan test in the application of a flash-based operations, to verify the device's manufacturing ID by the Provision Tool, of which first to define the device related configurations in the following procedures, commands circled in red for notation as shown;



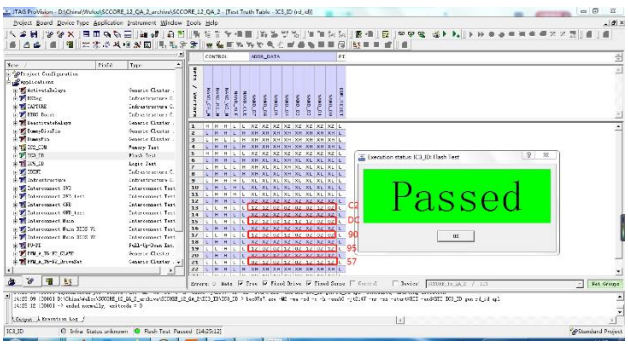
Picture 8. Validation of device ID tested by boundary scan

In Picture 9, a device ID is noted on its associated data bus in 8-bit binary coding and they are translated into HEX according to the spec. as shown in Picture 10;



Picture 9. Attentions made to data bus of a NAND flash memory for ID test

In Picture 10, the flash memory passed its ID test, of which is qualified as a KGD with respect to the device spec., evidentially the flash related data buss from D0 to D7 in 8-bits data stream as marked in HEX coding as 0xC2, 0xDC, 0x90, 0x95, 0x57 as if a wrong chip in contrast to the correct ID code as such C2, DC. 90, 95, 57 which is for the correct chip as shown in the truth table based report (TTR);



Picture 10. A device is passed on its ID code

2.6 Method of re-configuration of dies from Line of Centre (LOC) to Pin Grid Array (PGA)

Semiconductor back-end related process, for example, thin-film based technology, it sputters AL traces onto a layer of polyimide dielectric, etched out through photo-lithographic masking in order to remove excessive material and to build up Under-Bumps-Metal (UBM), crossing the via holes, may be blind or buried, through multiple layers of dimensional depositions and subsequently applying solder paste, it shall be re-flowed in making solder bumps, Al trances relocated from the original Line Of Centre (LOC) to a Pin Grid Array (PGA), this method is proposed based on a Design For Testing approach, illustrated on layers of deposition, and these layers are laid up step by step from aluminium, dielectric, UBM to passivation, as shown in Fig. 1;

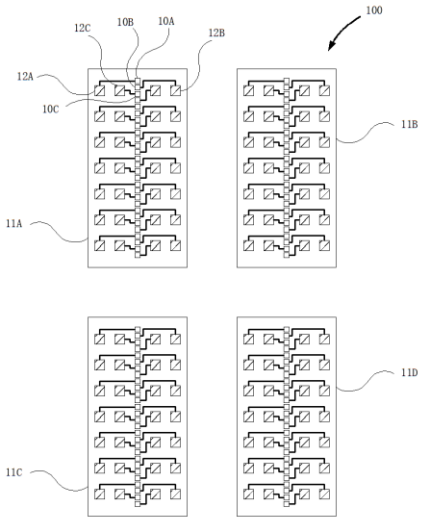


Fig. 1 Reconfigured Line of Centre (LOC) to Pin Grid Array (PGA)

2.7 Method of test signals embedded in the dicing streets and alleys

In Fig.1 is an overhead view of a typical rerouting sscheme for a portion of a wafer comprised of individual chips; for an example, during rerouting, the I/O pads of a chip such as the I/O pads (10A), (10B), (10C), etc., of the chip (11A), are fanned out into an area array comprised of bond pads (12A), (12B), (12C), etc. The bond pads (15), (25), (35), (40), (45), (50), (55), (60), (65), (4), (12A), (12B), (12C), etc., are orientated so that they match with the POD of a commercial JT2147 Quad-POD/JT37x7, plus a TAP controller (JTAG Technologist). Rerouting is typically used in the applications where components are mated together with either the interposer or substrate, but the IC and substrate are fabricated using different fabrication technologies (e.g., silicon or inorganic substrate). Often, the different fabrication technologies may have different resolution capabilities. Consequently, the I/O pads for the two components could be mated correctly in the application of dielectric layer, i.e., polyimide-based media not just for insolation but also for heat transfer in the consideration of stress relief is typically used when silicon chips are flip-chip bonded onto the MCM Substrates. The rerouting facilitates the proper orientation of the contacts (e.g., bond pads) of the chip with respect to the orientation of the bond pads of the substrate by using the photo-imageable polyimide, plus the Under-Bump Metallization (UBM) layer built-up to redefine the AL lines to the I/O pads (e.g., I/O pads (10A), (10B), (10C), etc. to an array of bond pads, such as bonds pads (12A), (12B), (12C) etc., that have a desired orientation. In this method, the bond pads may be finished with the UBM layer for subsequent integration of the chip, possibly with a mating assembly such as the substrate of an MCM and this process may be used, for instance to prepare a Wafer Scale CSP (WSCSP) as well. The first process step up the redistribution calling for “deposition” of a dielectric layer on the wafer to enhance the die related passivation through the AL traces used to reroute the pads to new locations, passing through blind and buried vias; however, with using Transverse Silicon Via (TSV) is also possible, they are to be filled up in the inner layers with non-conductive fill in the voids, while the ccopper filling is the most common practice for micro-vias; especially that is provided for excellent thermal conductivity among all of options. Thus, we apply this filling to all the inner layers to prevent the laser from reflection on the smooth surface. On the other hand, the origins of the TSV concept can be traced back to William Shockley's patent "Semiconductive Wafer and Method of Making the Same" filed in 1958 and granted in 1962, which was further developed by IBM researchers Merlin Smith and Emanuel Stern with their patent "Methods of Making Thru-Connections in Semiconductor Wafers" filed in 1964 and granted in 1967, and the latter describing a method for etching a hole through silicon, this to say TSV was not originally designed for 3D integration, and the first 3D chips based on TSV were invented later in the 1980s.

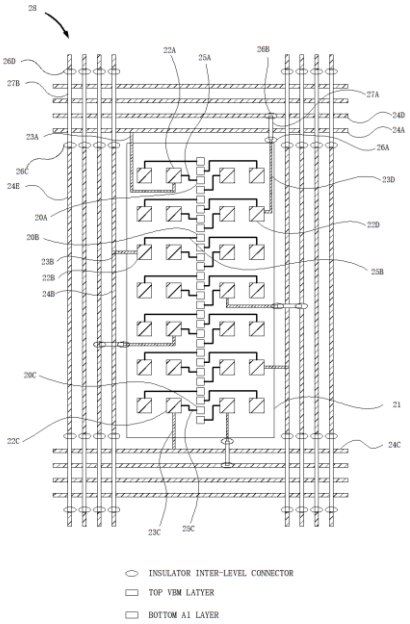


Fig. 2 Layout of 4x TAP signals across the die, embedded in the dicing streets and alleys

2.8 Method of signal buss assigned to the pins

In Fig. 2 is an overhead view of an embodiment of the present method in an application with a chip that has centrally located input and output pins, of which belong to a portion of a wafer comprised of a chip (21) having I/O pads in a center LOC layout. The wafer (28) may be comprised of many such chips as shown in the Fig. 2, the chip (21) is shown comprising I/O pads (20A), (20B), (20O), etc. As similarly illustrated in Fig 1, the I/O pads are shown rerouted to bond pads, such as bond pads (22A), (22B), (22C), etc., by rerouting leads (25A), (25B), (25C), etc. figure 2 also shows leads, such as leads (23A), (23B), (23C), etc., in accordance with an embodiment of the present method. In the embodiment shown in Fig 2, the leads (23A), (23B), (23C), etc., connect the bond pads (22A), (22B), (22C), etc., to individual bus lines (24A), (24B), (24C), etc., of a bus network. The bus network is formed in the dicing alleys between the chip (21) and the other chips (not shown) of the wafer (28). The re-configured chips of the wafer for boundary scan testing may be fabricated on the wafer in a similar row/ column as shown in Fig. 1. The other chips (not shown) of the wafer are also reconfigured in a similar manner to the bus lines of the bus network for boundary scan testing. In this way, wafer level boundary scan may be achieved by activating entire rows/columns of chips in "*parallel buss*" by using the bus lines (24A), (24B), (24C), etc., of the bus network. In this method, the number of leads that may be needed for a wafer level boundary scan is drastically reduced by sharing the bus lines (24A), (24B), (24C), etc., among the chips of the MCM. In accordance with an embodiment of the present method, the total number of wafer I/O connections that may be required to access 300 chips, positioned on a wafer, for boundary scan testing may be reduced from 1500 total I/O connections, if placed on a board (e.g., the 300 chips with connections per chip required for boundary scan testing), to 150 total I/O connections. The actual number of total I/O connections that may be required for boundary scan testing that will depend on the row and column configuration of the chips on the wafer and the number of I/O connections required in "*serial*" connections as said. In an embodiment of the present proposed method, the leads (23A), (23B), (23C), etc., and the bus lines (24A), (24B), (24C), etc., may be fabricated during the same process that forms the rerouting leads (25A), (25B), (25C), etc., and the bond pads (22A), (22B), (22C), etc. As shown in Fig. 2, and in some cases, a lead (23D), connecting a bond pad (22D), to a bus line (24D), may bypass a conducting portion on the wafer, such as a bus line (24A) and JTAG lines. In these cases, insulator inter-level connectors, such as connectors (26A), (26B), and a top crossover lead (27A) may be used to avoid shorting the bus line (24A) to the bus line (24D). Additionally, in cases where a bus line may cross another bus line, such as bus lines (24A) and (24E), a similar structure may be used, such as insulator inter-level connectors (26C) and (26D) and a top crossover lead (27B). In this way, the bus line (24A) may cross the bus line (24E) without making electrical contact. In the present method, the inter-level insulators e.g., connectors (26A) and (26B) may be formed during the rerouting process on the same level as done by the photo-imageable polyimide. The top crossover leads, such as top crossover leads (27A) and (27B), may be formed using the UBM level that is applied to the bond pads (not shown) during rerouting. In a preferred embodiment, a potential problem of having exposed leads corrode over time is eliminated by only using a top lead, such as top crossover leads (27A) and (27B) in the dicing alleys between the chips. When the individual chips are removed from the wafer (diced), these portions (e.g., the portions of the wafer between the chips) are removed. Consequently, the top leads are not left in connection of the chips and therefore do not pose a corrosion risk. Further, all the input and output connections to the bus lines are also

removed when the wafer is diced. Therefore, the AC/DC operating characteristics of the same chips are not affected by the proposed rerouting process. In Fig. 2, eight leads are required for boundary scan testing of the chip (21). More or less leads may be required for other types of chips. Nonetheless, the method of connecting the chip I/O connections to the bus lines for enabling wafer level boundary scan testing may remain the same, and they are exempted after dicing since traces within alleys and streets are removed, only bumping pads are left for flip chips with provision of the boundary scan required bumps, shown in a layout below;

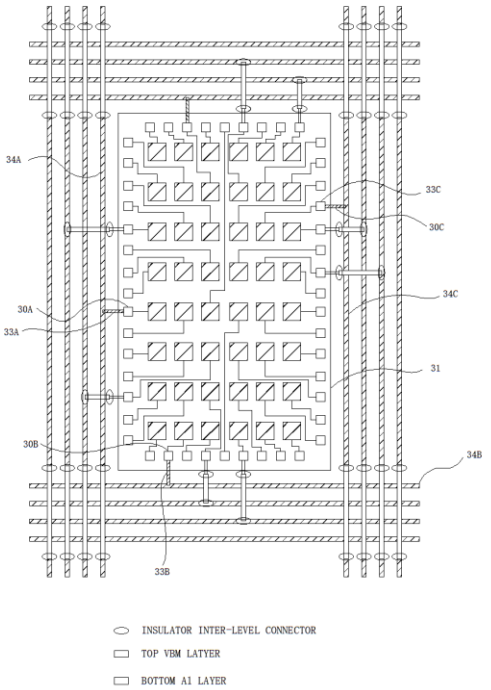


Fig. 3 Layout of signal buss to the assigned pin in the PGA configuration

2.9 Method of layout of dielectric and signal layers

In Fig. 3 shows another embodiment of the proposed method wherein a chip 31 has a peripheral layout f I/O bond pads. In this embodiment, sixteen leads are shown connecting the bond pads to the bus lines. Otherwise, the process of connecting the bond pads to the bus lines may be performed similarly to the process described above. In figure 3, the leads (33A), (33B), (33C), etc., are drawn connecting I/O pads, such as I/O pads (30A), (30B), (30C), etc., to bus lines, such as bus lines (34A), (34B), (34C), etc. In figure 2, the leads, such as the leads (24A), (24B), (24C), etc., are drawn connecting the bond pads to the bus lines. In one embodiment of the present method, the I/O pads may be used to connect the chip to the bus lines, and this typical rerouting fabrication process uses three levels of fabrication; it may utilize one or all three levels of a typical rerouting process to fabricate a wafer that facilitates wafer level boundary scan testing.

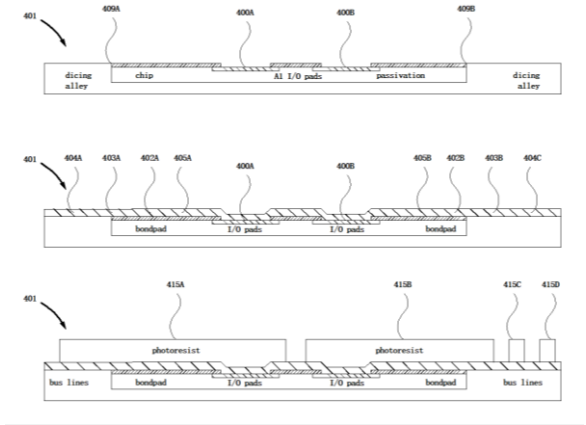


Fig. 4 (A-B-C) Cross-section view of dielectric layer lay-up

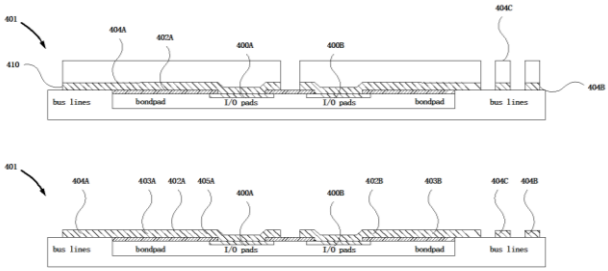


Fig. 4 (D-E) Cross-section view of Al layer lay up

In Fig. 4 **(**4A-4E) are side cross-sectional views illustrating the first fabrication level of a rerouting process in accordance with the present method. The above figures are side cross-sectional views illustrating a first fabrication level of a rerouting process in accordance with the present method, as such is that the first fabrication level of the rerouting process, a conductive layer is deposited on a chip (15), (25), (35), (40), (45), (50), (55), (60), (65), (6) and thereafter, is appropriately patterned. In figure 4, 4A shows a chip (401), that is part of a plurality of I/O pads. For instance, the chip (401) may have a

similar orientation as shown in figure 1 for the wafer 100 and the chip (11A). The chip (401) has I/O pads (400A), (400B) in an LOC layout. As shown, the chip is surrounded by dicing alleys (409A), (409B). As shown in Fig. (4B), during the first fabrication level of the rerouting process, aluminum may illustratively be deposited for forming (i) leads from I/O pads to bond pads, such as leads (405A), (405B); (ii) the bond pads, such as bond pads (402A), (402B); (iii) leads from bond pads to bus lines, such as leads (403A), (403B); and (iv) the bus lines, such as bus lines (404A), (404B), (404C). Features of (i) and (ii), stated above, are standard features in rerouting. Features (iii) and (iv), stated above, are features for facilitating boundary scan testing in accordance with an embodiment of the present method. In figure 4 (4B), the chip (401) is shown after coating with a conductive layer (410), that may illustratively be comprised of aluminum. The layer (410) may be deposited using a sputtering process or any other suitable deposition process. Other conductive materials, such as copper, etc., may be deposited in place of aluminum. The other conductive materials may also be deposited using a sputtering process or any other known suitable deposition process other than Al, Cu. AS shown, the conductive layer (410) is illustratively in contact with the I/O pads (400A), (400B) and extends into the dicing alleys (409A), (409B). figure 4 (4C) illustrates the next step wherein the conductive layer (410) (e.g., aluminum) is coated with a photoresist layer comprised of photoresist portions (415A), (415B), (415C), (415D). The photoresist portions are illustratively formed by first coating the chip 401 with a photoresist layer. Next, the photoresist layer is exposed through a mask and thereafter developed to form the photoresist portions. In Fig. 4 (4D), the conductive layer (410) is as shown etched, illustratively using a wet etch process, to electrically isolate the I/O pad (400A) from the I/O pad (400B), and to form electrically isolated bus lines (404B), (404C). Note that the bus line (404A) is not etched since in the embodiment shown, it is desired that the bus line (404A) be in electrical contact with the bond pad (402A) and the I/O pad (400A). In Fig. 4 (4E), the resulting chip (401) is shown after the photoresist portions (415A), (415B), 15C), (415D), as shown in Fig. 4 (4D) are stripped. As shown in figure 4 (4E), the lead (405A), the bond pad (402A), the bus lead (403A), and the bus line (404A) form one continuous connection between the I/O pad (400A), the bond pad (402A) and the bus line (404A). This type of connection is similar to the connection as shown in figure 4 between the I/O pad (20A), the lead (25A), the bond pad (22A), the lead (23A), and the bus line (24A). In one embodiment of the present method, only this form of continuous connection may be required for boundary scan testing. Consequently, no further fabrication levels may be required. Returning to Fig. 4 (4E), the I/O pad (400B) is connected to the bond pad (402B) through the I/O bond pad lead (405B). In the illustrative embodiment, it is desired that the bond pad (402B) is connected to the bus line (404B) through the lead (403B); however, a crossover is required over the bus line (404C); i.e., additional fabrication levels are required. This connection is similar to the connection shown in Fig. 4 between the bond pad (22D) and the bus line (24D). For forming this desired connection, levels two and three of the rerouting processes may be used to connect the bond pad (402B) to the bus line (404B), as discussed in more detail below.

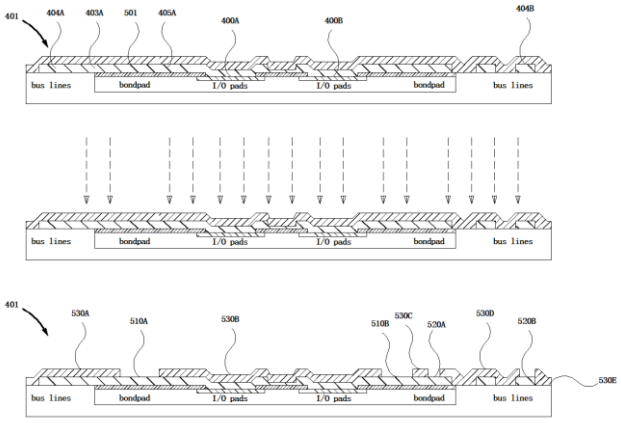


Fig.5 (5A-5C) side cross-sectional views of passivation

2.10 Method of layout of Under Metal Bumps (UBM)

In Fig. 5 (5A-5C) represents the present method, illustrates the second fabrication level of the rerouting process. In figure 5 (5A), the chip (401) is coated with a process compatible insulator to form a non-conductive layer (501), such as a photo-imageable polyimide layer. By the term process compatible, what intended is that an insulator be selected wherein fabrication (e.g., patterning) of the process compatible insulator not adversely affect the previous (first) level of fabrication. The layer (501) covers the leads (e.g., the leads (403A), (405A), etc., the I/O pads (e.g., the I/O pads (400A), (400B), etc.) and the bus lines (e.g., the bus lines (404A), (404B), etc.). It should be noted that although a photo-imageable polyimide is illustratively utilized for purposes of discussion

hereinafter as the layer (501), many other processable insulators may be suitably utilized for the layer (501) for address, data and control lines. For instance, there are also a broad base of non-photo sensitive polyimides that may be utilized. In addition, benzocy-clobutene (BCB*) is another processable insulator that has ssimilar properties to a polyimide and may be processed in a similar fashion as the polyimide. In figure (5B), a portion of the layer (501), illustratively a photo-imageable polyimide layer, is patterned illustratively through a photo mask so that only selected portions of the polyimide layer are exposed. In the embodiment shown in Fig. 5 (5B), a negative tone photo-imageable polyimide is illustratively used. For a negative tone photo-imageable polyimide, the exposed areas remain after development (e.g., a polyimide portion (530A) shown in figure 5 (5C). In an alternate embodiment (not shown), a positive tone photo imageable polyimide may be used in place of the negative tone photo-imageable polyimide. For a positive tone photo imageable polyimide, the exposed areas are removed during development. When using a positive tone photo-imageable polyimide, the photo mask should mask the portions of the photo-imageable polyimide that should remain after development (e.g., the polyimide portion 530A shown in Fig.5 (5C). In figure 5 (5), the photo-imageable polyimide layer is developed and cured to form polyimide portions (530A), (530B), (530C), (530D), (530E). As discussed in above, during development, portions of the polyimide layer are washed away to form the polyimide vias (510A), (510B) and cross over vias (520A), (520B) as well. Subsequently, The Under Bump Mmetallization (UBM) is a multilevel structure of sputtered Cr, Cr-Cu, and Cu thin films. The UBM provides an interface between the solder bump and the aluminum I/O pad, while the Cr provides adhesion to Al pad, Cu offers a solder wettable surface, shown in figure below.

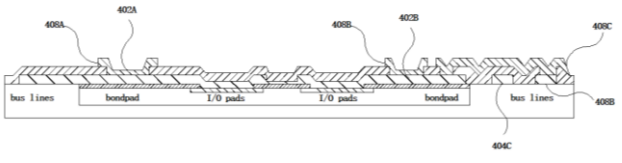


Fig. 6 Cross-sectional view of Under Metal Bumps (UBM)

In Fig. 6 illustratively shows the third fabrication level of the rerouting process in accordance with an embodiment of the present method. As typical in a rerouting process, an under-bump metallization layer comprised of under bump metallization portions (408A), (408B) are used to prepare the surface finish of the bond pads (402A), (402B) for subsequent solder bumping or solder-based assembly. In accordance with an embodiment of the present method, an under-bump metallization portion (408C) forms an electrical contact between the bond pad (402B) and the bus line (404B) while bypassing (e.g., not making electrical contact) the bus line (404C). This type of connection between the bond pad (402B) and the bus line (404B) is similar to the connection shown in Fig. 6 as such between the bond pad (22D) and the bus line (24D). While the above-described process illustratively shows a chip having an LOC layout with centrally located I/O pads, the present method may also illustratively be used wherein the I/O pads are in alternate LOC layouts, such as when the I/O pads are in a peripheral layout. In general, the method may be applicable to all chip wafers, and the method is applied wherein rerouting is part of the typical fabrication process for a chip's I/O's are rerouted for flip-chip bonding to an MCM substrate.

3. Results

3.1 The result of programming flash memory on a die

In this proposal, we have simulated a typical Flash mmemory as the test specimen, undergoing JTAG's flash memory cluster test on a wafer, and to program this flash memory on a flip-chip, data sheets are modelled by the JTAG's Provision software tool, to conduct the self-test required Device Configuration Format, test procedures are depicted in Fig. 7;

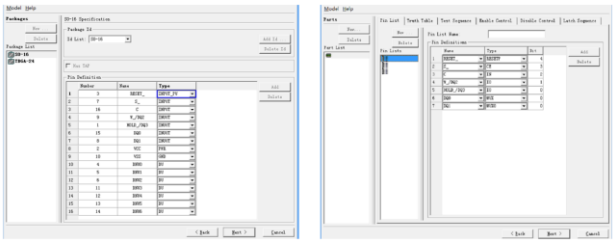


Fig. 7 Development of the cluster-based boundary scan testing and In-System-Programming (ISP)

3.2 The result of Self-test-based Carriage Return Checking

When the Flash is emulated along with its hosted MCU in extension of the internal buss, first to test the boundary scan

required Infrastructure test according to the MCU's pre-defined BSDL file, to read, write, erase and blank check, and/or the Carriage Return Checking (CRC) in the core of the MCU. Typically, it checks a set of internal signals as if the MCU is running polynomial equations, known to the seeding of the internal test, and subsequently to generate a fixed checksum at the end of self-test as shown in Fig. 8;

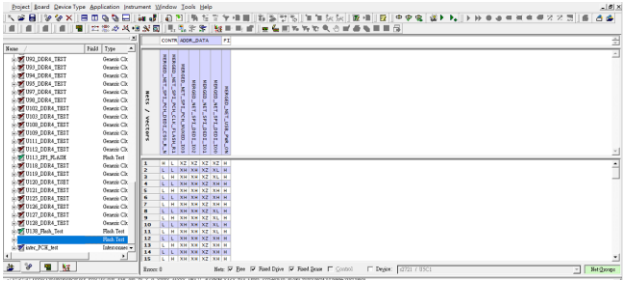


Fig. 8 Flash memory buss under testing by Boundary Scan based Cluster Test

3.3 The result in Truth Table based Vector Analysis

When the cluster test passes the Flash memory, it is qualified for In-System-Programming (ISP), and the truth table illustrated the test vectors in Fig. 9, it exhibits all buss of this flash memory possibly in a host of a MCU or a System-On-Chip (SOC) as follows:

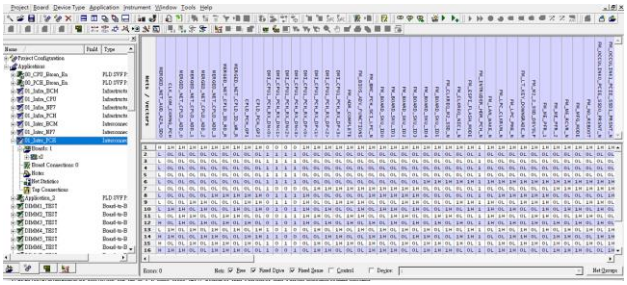


Fig. 9 Interconnection test checking the MCU related data, address and control buss

3.4 The result of test sequence and programming

A system chip like an MCM, it has plural dices, and one of which may be a flash memory, allowed to read, write and fetch the data in the test sequence of Fig. 10, 11, 12 and 13 in four steps; thereafter to load image memory in binary coding, next to perform boundary scan based cluster test to execute "erase", "blank check", "write" and "verification" and debugging, depicted as follows:

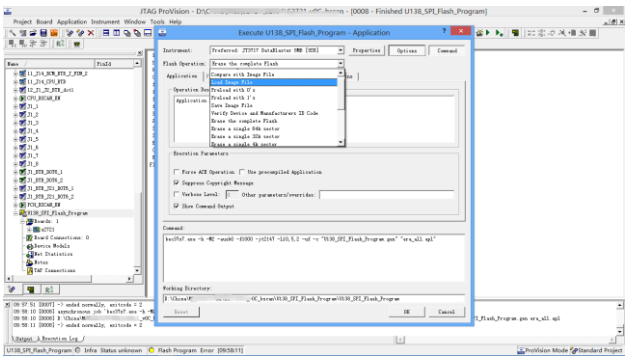


Fig. 10 step 1: Flash memory loading image files

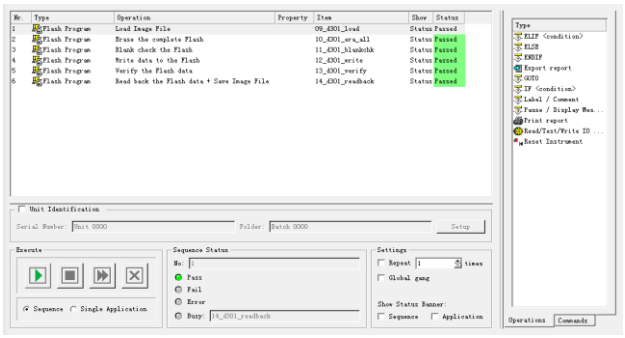


Fig. 11 step 2: Flash memory under erasing, blank checking, writing and verification

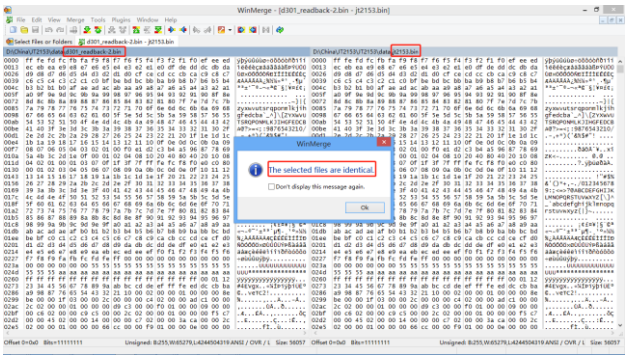


Fig. 12 step 3: Partitioned Flash Memory in blocks

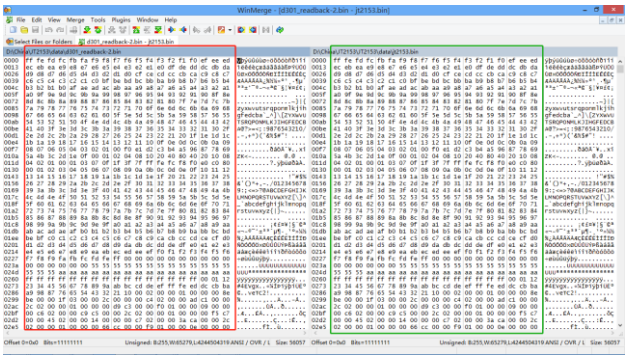


Fig. 13 Step 4: To compare the error memory bits with the correct ones

3.5 The result of system level test on Known Good Dies

This method and setup have made possible to check bad dies against the "gold die" in the paired modules, and the following figures illustrate the twin-MCMs based setup, to test the dies on per pins and nets base, with respect to each other's mirror images, they are 1X, 2X and 3X of the MCM-X in contrast to dies numbered as 1Y, 2Y and 3Y of the paired MCM-Y; defective dice reveal their faulty boundary scan cell in error bits, as shown in Figure 14 when the MCM-Y is identical to MCM-X, and that means all flip-chip based dies are Known-Good-Dies are checked and proven on a truth table in Fig. 14;

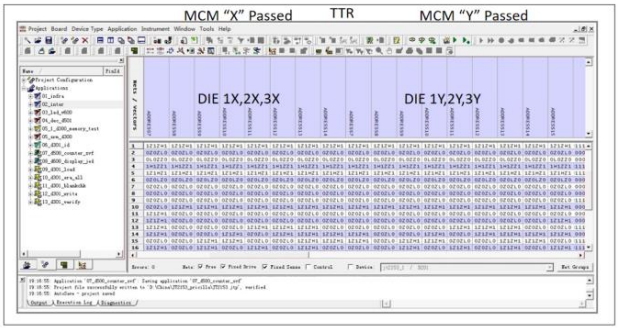


Fig. 14: passed dies validated by the gold dies in a paired MCM-X and Y

4. Conclusions

- This paper proposes a new way to possibly embed the boundary scan test signals into the rerouted channels of the wafer through thin-film based process, by taking advantages of uncut dies with available dicing streets and alleys, further to implant test signals into each individual die, and to reach their perspective bumps, not only redefine existing pads but also fan them out for flip-chips.
- Since today's ICs most likely equipped with the boundary scan cells on each die, and the thin-film process is getting mature, giving birth to the MCM with KGD within the assembly is made possible;
- Future works towards chip-lets assembly, proposed by Dr. Shang Yong Hou on the subject of "Interposer Technology, the past, current and future", made a breakthrough in small ides, so called "chiplets", and that shall significantly yield in die in expression of Exp ($-D_0$ *A) where "A" is representing downsized area, and this thesis shall realize the CoWoS related works in the area of semiconductor-based systems.

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矽晶圓後段之封裝與測試及裸晶之研發

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摘　要

半導體晶圓後處理以細薄膜技術，重新分置信號凸球於井字型分佈，並且在切割分界中植入邊界掃描測試用信號線，以期在生產覆晶片過程中，同時達到該晶片自我檢測的目標。為了在封裝前的晶圓上設計並製作好模具(KGD)，它要求 I/O 焊盤通過通道化的重佈線/重分佈過程以扇形展開，從而按照標準的邊界掃描測試（BST）驅動和感測每個晶片作為反對傳統的 AC / DC 類型的模擬測試，以符合 IEEE 1149 標準，要加強每個 IC，這是提出的生產 KGD 在晶圓上的批次處理模式的方法，而且，在製造倒裝晶片時，它們很容易被碰撞、邊界掃描測試和切片，而無需探測、使用插座等，這是一種擴展性的解決方案，可以在封裝之前鑒定和驗證未知的晶片。

關鍵詞：覆晶、邊界掃描、捷泰克、裸晶測試